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| EXAMINER | |
|---|---|
| YIGDALL, MICHAEL J | |

| ART UNIT | PAPER NUMBER |
|---|---|
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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/998,629 | MORRISON ET AL. | |
| | Examiner | Art Unit | |
| | Michael J. Yigdall | 2192 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *27-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *27-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____

## DETAILED ACTION

1. This Office action is responsive to Applicant's submission filed on May 22, 2006. Claims 27-36 are now pending.

### *Response to Arguments*

2. Applicant's arguments with respect to the recited management processors (remarks, pages 10-12) were fully considered and are persuasive. Therefore, the rejections of claims 27-29 under 35 U.S.C. 103(a) are withdrawn. However, upon further consideration, new rejections under 35 U.S.C. 103(a) are made in view of Evans, as set forth below.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 30 and 31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Claim 30 recites an operation that is performed "upon recognizing that the firmware of the first cell is corrupt." However, the claim recites that the firmware of the first cell is "errored firmware" rather than corrupt firmware, and further recites, "recognizing that the firmware in the nonvolatile memory system of the first cell is errored." Accordingly, the term "corrupt" is treated as "errored" in the rejection of claim 30 below.

Claim 31 recites, "recognizing that the firmware in the nonvolatile memory system of the first cell is corrupt." However, the claim recites that the firmware of the first cell is "errored firmware" rather than corrupt firmware, and further recites an operation that is performed "upon recognizing that the firmware of the first cell is errored." Accordingly, the term "corrupt" is treated as "errored" in the rejection of claim 31 below.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 27-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pub. No. 2002/0091807 to Goodman (art of record, "Goodman") in view of U.S. Patent No. 5,163,052 to Evans et al. (now made of record, "Evans") in view of U.S. Patent No. 6,665,813 to Forsman et al. (art of record, "Forsman").

With respect to claim 27 (currently amended), Goodman discloses a high-availability cellular computer system capable of automatically updating firmware in cells of the system (see, for example, nodal system 100 in FIG. 1 and the abstract), the system comprising:

a high speed interconnect (see, for example, communication interface 42 in FIG. 1); and

a first cell and a second cell (see, for example, nodes 20 and 40 in FIG. 1), each cell comprising at hardware level:

at least one processor of the cell coupled to at least one random-access memory subsystem of the cell (see, for example, processor 22 and RAM 26 in FIG. 1),

at least one nonvolatile memory system coupled to the at least one processor of the cell (see, for example, programmable memory 24 in FIG. 1), and

a high-speed interconnect interface coupling the at least one processor of the cell to the high speed interconnect (see, for example, paragraph 0017, lines 14-21).

Goodman does not expressly disclose a management interconnect, and does not expressly disclose each cell comprising at hardware level:

a management processor of the cell coupled to a nonvolatile memory for management code of the cell, and

an interface coupling the management processor of the cell to the management interconnect.

However, in an analogous art, Evans discloses a cellular computer system (see, for example, computer system 200 in FIG. 2) that comprises a high speed interconnect (see, for example, processor-memory bus 216 in FIG. 2 and column 3, lines 1-4) and a management interconnect (see, for example, serial diagnostics bus 218 in FIG. 2 and column 3, lines 5-7). Each cell comprises, at the hardware level, a management processor with a nonvolatile memory storing management code (see, for example, microcontroller unit 226 in FIG. 2 and column 3, lines 9-14), and an interface coupling the management processor to the management interconnect (see, for example, column 3, lines 5-7).

The management processors and the management interconnect are operable independently of the processors to perform management functions such as diagnostics and

corrective actions (see, for example, column 1, lines 55-65 and column 3, lines 42-58), even when the processors fail (see, for example, column 1, lines 20-26).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate management processors and a management interconnect into the system of Goodman, such as taught in Evans, so as to perform management functions independently of the processors.

Goodman in view of Evans further discloses:

wherein the nonvolatile memory subsystem of the first cell has recorded therein errored firmware selected from the group consisting of outdated or corrupt firmware (see, for example, paragraph 0021, lines 1-9 and 16-18, which shows a node that has outdated firmware), and the nonvolatile memory subsystem of the second cell has recorded therein valid firmware (see, for example, paragraph 0021, lines 10-15, which shows a node that has valid firmware); and

wherein the first cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the first cell is errored firmware (see, for example, paragraph 0025, lines 2-13, which shows that the first node determines that its firmware is outdated) and, upon recognizing that the firmware of the first cell is errored, for transmitting over the management interconnect a request for valid firmware to the second cell (see, for example, paragraph 0027, lines 3-6, which shows that the first node transmits a request for the valid firmware to the second node), and for updating the nonvolatile memory system of the first cell with valid firmware (see, for example, paragraph 0027, lines 10-13, which shows that the first node updates its firmware with the valid firmware);

wherein the second cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the second cell is valid (see, for example, paragraph 0023, lines 7-14, which shows that the second node determines that its firmware is valid); and

wherein the management code of the second cell comprises machine readable code to receive a request for valid firmware and, in response thereto, to transmit an acknowledgement via the manageability system interconnect (see, for example, paragraph 0023, lines 7-14, which shows that the second cell receives a request for valid firmware and transmits an acknowledgement in response), to enable the high speed interconnect (see, for example, paragraph 0017, lines 14-21, which shows that the high speed interconnect is enabled); and to transmit the firmware in the nonvolatile memory system of the second cell to the first cell via the high speed interconnect (see, for example, paragraph 0027, lines 6-8, which shows that the second node transmits its firmware to the first node).

Goodman in view of Evans does not expressly disclose that it is the management processor of each cell that performs the above firmware operations.

However, in an analogous art, Forsman discloses a management processor (see, for example, service processor 224 in FIG. 2 and column 3, lines 60-64) that coordinates the operations for updating firmware (see, for example, column 4, lines 2-3). Like the management processors of Evans, the management processor of Forsman operates even in the event of a system failure (see, for example, column 3, line 64 to column 4, line 1), such as corrupt firmware (see, for example, column 1, lines 24-29). Forsman discloses recognizing whether the firmware is corrupt (see, for example, column 1, lines 50-55), and recovering the firmware if necessary (see, for example, column 6, lines 16-28).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the management processors in the system of Goodman and Evans perform the firmware operations, such as taught in Forsman, so as to provide for recovery in the event of corrupt firmware.

With respect to claim 28 (currently amended), the rejection of claim 27 is incorporated, and Goodman in view of Evans in view of Forsman further discloses that the errored firmware is corrupt firmware (see, for example, Forsman, column 1, lines 50-55, which shows determining that the firmware is corrupt).

With respect to claim 29 (currently amended), the rejection of claim 27 is incorporated, and Goodman in view of Evans in view of Forsman further discloses that the errored firmware is outdated firmware (see, for example, paragraph 0025, lines 2-13, which shows determining that the firmware is outdated).

With respect to claim 30 (new), Goodman discloses a high-availability cellular computer system capable of automatically updating firmware in cells of the system (see, for example, nodal system 100 in FIG. 1 and the abstract), the system comprising:

a physical high speed interconnect (see, for example, communication interface 42 in FIG. 1); and

a first cell and a second cell (see, for example, nodes 20 and 40 in FIG. 1), each cell comprising at least one physical processor (see, for example, processor 22 in FIG. 1) coupled to

at least one physical random-access memory subsystem of the cell (see, for example, RAM 26 in FIG. 1),

at least one physical nonvolatile memory system of the cell (see, for example, programmable memory 24 in FIG. 1), and

a high-speed interconnect interface (see, for example, paragraph 0017, lines 14-21).

Goodman does not expressly disclose a physical manageability interconnect, and does not expressly disclose each cell comprising at least one physical processor coupled to:

a cell manageability subsystem coupled to the manageability interconnect, the cell manageability subsystem comprising a cell manageability processor.

However, in an analogous art, Evans discloses a cellular computer system (see, for example, computer system 200 in FIG. 2) that comprises a physical high speed interconnect (see, for example, processor-memory bus 216 in FIG. 2 and column 3, lines 1-4) and a physical manageability interconnect (see, for example, serial diagnostics bus 218 in FIG. 2 and column 3, lines 5-7). Each cell comprises at least one physical processor (see, for example, CPU 220 in FIG. 2) coupled to a cell manageability subsystem that is coupled to the manageability interconnect and that comprises a cell manageability processor (see, for example, microcontroller unit 226 in FIG. 2 and column 3, lines 5-14).

The manageability processors and the manageability interconnect are operable independently of the processors to perform manageability functions such as diagnostics and corrective actions (see, for example, column 1, lines 55-65 and column 3, lines 42-58), even when the processors fail (see, for example, column 1, lines 20-26).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate manageability processors and a manageability interconnect

into the system of Goodman, such as taught in Evans, so as to perform manageability functions independently of the processors.

Goodman in view of Evans further discloses:

wherein the high-speed interconnect interface of the first cell and the second cell is coupled to the high speed interconnect (see, for example, paragraph 0017, lines 14-21); and

wherein the nonvolatile memory subsystem of the first cell has recorded therein errored firmware (see, for example, paragraph 0021, lines 1-9 and 16-18, which shows a node that has outdated firmware), and the nonvolatile memory subsystem of the second cell has recorded therein valid firmware (see, for example, paragraph 0021, lines 10-15, which shows a node that has valid firmware); and

wherein the first cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the first cell is errored (see, for example, paragraph 0025, lines 2-13, which shows that the first node determines that its firmware is outdated) and, upon recognizing that the firmware of the first cell is corrupt, for updating the nonvolatile memory system of the first cell with firmware copied from a cell having valid firmware (see, for example, paragraph 0027, lines 10-13, which shows that the first node updates its firmware with the valid firmware);

wherein the second cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the second cell is valid (see, for example, paragraph 0023, lines 7-14, which shows that the second node determines that its firmware is valid); and

wherein the cell manageability processor of the second cell contains machine readable code to receive an update message via the manageability system interconnect and, in response

thereto, to transmit an acknowledgement via the manageability system interconnect (see, for example, paragraph 0023, lines 7-14, which shows that the second cell receives a request for valid firmware and transmits an acknowledgement in response), to enable the high speed interconnect (see, for example, paragraph 0017, lines 14-21, which shows that the high speed interconnect is enabled); and to transmit the firmware in the nonvolatile memory system of the second cell to the first cell via the high speed interconnect (see, for example, paragraph 0027, lines 6-8, which shows that the second node transmits its firmware to the first node).

Goodman in view of Evans does not expressly disclose that it is the manageability processor of each cell that performs the above firmware operations.

However, in an analogous art, Forsman discloses a manageability processor (see, for example, service processor 224 in FIG. 2 and column 3, lines 60-64) that coordinates the operations for updating firmware (see, for example, column 4, lines 2-3). Like the manageability processors of Evans, the manageability processor of Forsman operates even in the event of a system failure (see, for example, column 3, line 64 to column 4, line 1), such as corrupt firmware (see, for example, column 1, lines 24-29). Forsman discloses recognizing whether the firmware is corrupt (see, for example, column 1, lines 50-55), and recovering the firmware if necessary (see, for example, column 6, lines 16-28).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the manageability processors in the system of Goodman and Evans perform the firmware operations, such as taught in Forsman, so as to provide for recovery in the event of corrupt firmware.

With respect to claim 31 (new), Goodman discloses a high-availability cellular computer system capable of automatically updating firmware in cells of the system (see, for example, nodal system 100 in FIG. 1 and the abstract), the system comprising:

a physical high speed interconnect (see, for example, communication interface 42 in FIG. 1); and

a first cell and a second cell (see, for example, nodes 20 and 40 in FIG. 1), each cell comprising at least one physical processor (see, for example, processor 22 in FIG. 1) coupled to

at least one physical random-access memory subsystem of the cell (see, for example, RAM 26 in FIG. 1),

at least one physical nonvolatile memory system of the cell (see, for example, programmable memory 24 in FIG. 1), and

a high-speed interconnect interface (see, for example, paragraph 0017, lines 14-21).

Goodman does not expressly disclose a physical manageability interconnect, and does not expressly disclose each cell comprising at least one physical processor coupled to:

a cell manageability subsystem coupled to the manageability interconnect, the cell manageability subsystem comprising a cell manageability processor.

However, in an analogous art, Evans discloses a cellular computer system (see, for example, computer system 200 in FIG. 2) that comprises a physical high speed interconnect (see, for example, processor-memory bus 216 in FIG. 2 and column 3, lines 1-4) and a physical manageability interconnect (see, for example, serial diagnostics bus 218 in FIG. 2 and column 3, lines 5-7). Each cell comprises at least one physical processor (see, for example, CPU 220 in

FIG. 2) coupled to a cell manageability subsystem that is coupled to the manageability interconnect and that comprises a cell manageability processor (see, for example, microcontroller unit 226 in FIG. 2 and column 3, lines 5-14).

The manageability processors and the manageability interconnect are operable independently of the processors to perform manageability functions such as diagnostics and corrective actions (see, for example, column 1, lines 55-65 and column 3, lines 42-58), even when the processors fail (see, for example, column 1, lines 20-26).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate manageability processors and a manageability interconnect into the system of Goodman, such as taught in Evans, so as to perform manageability functions independently of the processors.

Goodman in view of Evans further discloses:

wherein the high-speed interconnect interface of the first cell and the second cell is coupled to the high speed interconnect (see, for example, paragraph 0017, lines 14-21); and

wherein the nonvolatile memory subsystem of the first cell has recorded therein errored firmware (see, for example, paragraph 0021, lines 1-9 and 16-18, which shows a node that has outdated firmware), and the nonvolatile memory subsystem of the second cell has recorded therein valid firmware (see, for example, paragraph 0021, lines 10-15, which shows a node that has valid firmware); and

wherein the first cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the first cell is corrupt (see, for example, paragraph 0025, lines 2-13, which shows that the first node determines that its firmware is outdated) and, upon

recognizing that the firmware of the first cell is errored, for updating the nonvolatile memory system of the first cell with firmware copied from a cell having valid firmware (see, for example, paragraph 0027, lines 10-13, which shows that the first node updates its firmware with the valid firmware);

wherein the second cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the second cell is valid (see, for example, paragraph 0023, lines 7-14, which shows that the second node determines that its firmware is valid); and

wherein the cell manageability processor of the second cell contains machine readable code to receive an update message via the manageability system interconnect (see, for example, paragraph 0023, lines 7-14, which shows that the second cell receives a request for valid firmware) and, in response thereto, for transmitting the firmware in the nonvolatile memory system of the second cell to the first cell via the manageability interconnect (see, for example, paragraph 0027, lines 6-8, which shows that the second node transmits its firmware to the first node).

Goodman in view of Evans does not expressly disclose that it is the manageability processor of each cell that performs the above firmware operations, and does not expressly disclose that the firmware is transmitted via the manageability interconnect.

However, in an analogous art, Forsman discloses a manageability processor (see, for example, service processor 224 in FIG. 2 and column 3, lines 60-64) that coordinates the operations for updating firmware (see, for example, column 4, lines 2-3). The firmware is updated via a manageability bus (see, for example, service processor bus 228 in FIG.2 and column 4, lines 2-3). Like the manageability processors of Evans, the manageability processor

of Forsman operates even in the event of a system failure (see, for example, column 3, line 64 to column 4, line 1), such as corrupt firmware (see, for example, column 1, lines 24-29). Forsman discloses recognizing whether the firmware is corrupt (see, for example, column 1, lines 50-55), and recovering the firmware if necessary (see, for example, column 6, lines 16-28).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the manageability processors in the system of Goodman and Evans perform the firmware operations, and that the firmware is transmitted via the manageability interconnect, such as taught in Forsman, so as to provide for recovery in the event of corrupt firmware.

With respect to claim 32 (new), Goodman discloses a high-availability cellular computer system capable of automatically updating firmware in cells of the system (see, for example, nodal system 100 in FIG. 1 and the abstract), the system comprising:

a high speed interconnect (see, for example, communication interface 42 in FIG. 1);

a first cell and a second cell (see, for example, nodes 20 and 40 in FIG. 1), each cell comprising at hardware level:

at least one processor of the cell coupled to at least one random-access memory subsystem of the cell (see, for example, processor 22 and RAM 26 in FIG. 1),

at least one nonvolatile memory system coupled to the at least one processor of the cell (see, for example, programmable memory 24 in FIG. 1),

a high-speed interconnect interface coupling the at least one processor of the cell to the high speed interconnect (see, for example, paragraph 0017, lines 14-21),

Goodman does not expressly disclose a manageability interconnect, and does not expressly disclose each cell comprising at hardware level:

a cell manageability processor coupled to the manageability interconnect;

However, in an analogous art, Evans discloses a cellular computer system (see, for example, computer system 200 in FIG. 2) that comprises a high speed interconnect (see, for example, processor-memory bus 216 in FIG. 2 and column 3, lines 1-4) and a manageability interconnect (see, for example, serial diagnostics bus 218 in FIG. 2 and column 3, lines 5-7). Each cell comprises, at the hardware level, a manageability processor (see, for example, microcontroller unit 226 in FIG. 2 and column 3, lines 9-14) that is coupled to the manageability interconnect (see, for example, column 3, lines 5-7).

The manageability processors and the manageability interconnect are operable independently of the processors to perform manageability functions such as diagnostics and corrective actions (see, for example, column 1, lines 55-65 and column 3, lines 42-58), even when the processors fail (see, for example, column 1, lines 20-26).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate manageability processors and a manageability interconnect into the system of Goodman, such as taught in Evans, so as to perform manageability functions independently of the processors.

Goodman in view of Evans further discloses:

wherein the high-speed interconnect interface of the first cell and the second cell is coupled to the high speed interconnect (see, for example, paragraph 0017, lines 14-21); and

wherein the nonvolatile memory subsystem of the first cell has recorded therein corrupt firmware (see, for example, paragraph 0021, lines 1-9 and 16-18, which shows a node that has outdated firmware), and the nonvolatile memory subsystem of the second cell has recorded therein valid firmware (see, for example, paragraph 0021, lines 10-15, which shows a node that has valid firmware); and

wherein the first cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the first cell is corrupt (see, for example, paragraph 0025, lines 2-13, which shows that the first node determines that its firmware is outdated) and, upon recognizing that the firmware of the first cell is corrupt, for updating the nonvolatile memory system of the first cell with firmware copied from a cell having valid firmware (see, for example, paragraph 0027, lines 10-13, which shows that the first node updates its firmware with the valid firmware); and

wherein the second cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the second cell is valid (see, for example, paragraph 0023, lines 7-14, which shows that the second node determines that its firmware is valid); and

wherein the management processor of the second cell has machine readable code to receive an update message via the manageability system interconnect and, in response thereto, to transmit an acknowledgement via the manageability system interconnect (see, for example, paragraph 0023, lines 7-14, which shows that the second cell receives a request for valid firmware and transmits an acknowledgement in response), to enable the high speed interconnect (see, for example, paragraph 0017, lines 14-21, which shows that the high speed interconnect is enabled); and to transmit the firmware in the nonvolatile memory system of the second cell to the

first cell via the high speed interconnect (see, for example, paragraph 0027, lines 6-8, which shows that the second node transmits its firmware to the first node).

Goodman in view of Evans does not expressly disclose that the firmware is updated because it is corrupt and that it is the manageability processor of each cell that performs the above firmware operations.

However, in an analogous art, Forsman discloses a manageability processor (see, for example, service processor 224 in FIG. 2 and column 3, lines 60-64) that coordinates the operations for updating firmware (see, for example, column 4, lines 2-3). Like the manageability processors of Evans, the manageability processor of Forsman operates even in the event of a system failure (see, for example, column 3, line 64 to column 4, line 1), such as corrupt firmware (see, for example, column 1, lines 24-29). Forsman discloses recognizing whether the firmware is corrupt (see, for example, column 1, lines 50-55), and recovering the firmware if necessary (see, for example, column 6, lines 16-28).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the manageability processors in the system of Goodman and Evans perform the firmware operations, such as taught in Forsman, so as to provide for recovery in the event of corrupt firmware.

With respect to claim 33 (new), Goodman discloses a method for updating firmware in a cellular, high availability, computing system (see, for example, nodal system 100 in FIG. 1 and the abstract) comprising:

providing a plurality of cells of a cellular computing system (see, for example, nodes 20 and 40 in FIG. 1), where each cell has firmware (see, for example, programmable memory 24 in FIG. 1 and paragraph 0019, lines 3-9) and comprises:

at least one processor (see, for example, processor 22 in FIG. 1),

a random-access memory coupled to the at least one processor (see, for example, RAM 26 in FIG. 1), and

a high-speed interconnect interface (see, for example, communication interface 42 in FIG. 1 and paragraph 0017, lines 14-21);

Goodman does not expressly disclose that each cell comprises a management processor.

However, in an analogous art, Evans discloses a cellular computer system (see, for example, computer system 200 in FIG. 2). Each cell comprises a management processor (see, for example, microcontroller unit 226 in FIG. 2 and column 3, lines 5-14). The management processors are operable independently of the processors to perform management functions such as diagnostics and corrective actions (see, for example, column 1, lines 55-65 and column 3, lines 42-58), even when the processors fail (see, for example, column 1, lines 20-26).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate management processors into the system of Goodman, such as taught in Evans, so as to perform management functions independently of the processors.

Goodman in view of Evans further discloses:

determining a first cell of the plurality of cells having errored firmware (see, for example, paragraph 0021, lines 1-9 and 16-18, which shows a first node that has outdated firmware), and

an update cell of the plurality of cells having desired firmware (see, for example, paragraph 0021, lines 10-15, which shows an update node that has desired firmware);

sending a firmware update request from the management processor of the update cell over a management interconnect to the management processor of the first cell (see, for example, paragraph 0023, lines 7-14, which shows sending a firmware update request, and see, for example, Evans, serial diagnostics bus 218 in FIG. 2 and column 3, lines 5-7, which shows a management interconnect); and

transmitting the desired firmware from the update cell through a high-speed interconnect into the first cell (see, for example, paragraph 0027, lines 6-8, which shows transmitting the desired firmware to the first node);

wherein the high-speed interconnect is distinct from the management interconnect (see, for example, Evans, FIG. 2 and column 3, lines 1-7, which shows that processor-memory bus 216 is distinct from serial diagnostics bus 218), and during normal operation of the computing system is used for communications between a plurality of cells of the computing system (see, for example, paragraph 0017, lines 14-21, which shows that the high-speed interconnect is used for communications among nodes).

Goodman in view of Evans does not expressly disclose that it is the management processor of each cell that performs the above firmware operations.

However, in an analogous art, Forsman discloses a management processor (see, for example, service processor 224 in FIG. 2 and column 3, lines 60-64) that coordinates the operations for updating firmware (see, for example, column 4, lines 2-3). Like the management processors of Evans, the management processor of Forsman operates even in the event of a

system failure (see, for example, column 3, line 64 to column 4, line 1), such as corrupt firmware (see, for example, column 1, lines 24-29). Forsman discloses recognizing whether the firmware is corrupt (see, for example, column 1, lines 50-55), and recovering the firmware if necessary (see, for example, column 6, lines 16-28).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the management processors in the system of Goodman and Evans perform the firmware operations, such as taught in Forsman, so as to provide for recovery in the event of corrupt firmware.

With respect to claim 34 (new), the rejection of claim 33 is incorporated, and Goodman in view of Evans in view of Forsman further discloses that the errored firmware is firmware selected from the group consisting of missing firmware, corrupt firmware, and outdated firmware (see, for example, paragraph 0025, lines 2-13, which shows determining that the firmware is outdated).

With respect to claim 35 (new), the rejection of claim 33 is incorporated, and Goodman in view of Evans in view of Forsman further discloses:

when the update cell receives over the management interconnect an acknowledgment of the firmware update request from the first cell prior to transmitting the desired firmware to the first cell (see, for example, paragraph 0023, lines 7-14, which shows receiving an acknowledgement prior to transmitting the desired firmware).

With respect to claim 36 (new), the rejection of claim 35 is incorporated, and Goodman in view of Evans in view of Forsman further discloses that the step of determining a first cell of

the plurality of cells having errored firmware is performed by the management processors of the cells (see, for example, Forsman, column 4, lines 2-3, which shows that the management processors coordinate the operations for updating firmware).

7. Claims 27-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goodman in view of U.S. Patent No. 6,684,343 to Bouchier et al. (now made of record, "Bouchier '343") in view of Forsman.

The Bouchier '343 reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another;" (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

The examiner anticipates that this rejection will be overcome by a proper showing under 35 U.S.C. 103(c) that the reference is disqualified as prior art in a rejection under 35 U.S.C.

103(a). Accordingly, to expedite prosecution, one representative claim is presented below to illustrate the subject matter disclosed in the reference.

With respect to claim 32 (new), for example, Goodman discloses a high-availability cellular computer system capable of automatically updating firmware in cells of the system (see, for example, nodal system 100 in FIG. 1 and the abstract), the system comprising:

a high speed interconnect (see, for example, communication interface 42 in FIG. 1);

a first cell and a second cell (see, for example, nodes 20 and 40 in FIG. 1), each cell comprising at hardware level:

at least one processor of the cell coupled to at least one random-access memory subsystem of the cell (see, for example, processor 22 and RAM 26 in FIG. 1),

at least one nonvolatile memory system coupled to the at least one processor of the cell (see, for example, programmable memory 24 in FIG. 1),

a high-speed interconnect interface coupling the at least one processor of the cell to the high speed interconnect (see, for example, paragraph 0017, lines 14-21),

Goodman does not expressly disclose a manageability interconnect, and does not expressly disclose each cell comprising at hardware level:

a cell manageability processor coupled to the manageability interconnect;

However, in an analogous art, Bouchier '343 discloses a cellular computer system (see, for example, FIG. 1) that comprises a high speed interconnect (see, for example, column 4, lines 35-40) and a manageability interconnect (see, for example, column 4, lines 13-21). Each cell comprises, at the hardware level, a manageability processor (see, for example, cell microcontroller 304 in FIG. 1 and column 4, lines 8-13) that is coupled to the manageability

interconnect (see, for example, column 4, lines 13-21). The manageability processors and the manageability interconnect are able to update the firmware of a cell (see, for example, column 5, lines 40-45), even when the cell is not part of a partition and is unbootable (see, for example, column 3, lines 14-17).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate manageability processors and a manageability interconnect into the system of Goodman, such as taught in Bouchier '343, so as to update the firmware of a cell even when it is unbootable.

Goodman in view of Bouchier '343 further discloses:

wherein the high-speed interconnect interface of the first cell and the second cell is coupled to the high speed interconnect (see, for example, paragraph 0017, lines 14-21); and

wherein the nonvolatile memory subsystem of the first cell has recorded therein corrupt firmware (see, for example, paragraph 0021, lines 1-9 and 16-18, which shows a node that has outdated firmware), and the nonvolatile memory subsystem of the second cell has recorded therein valid firmware (see, for example, paragraph 0021, lines 10-15, which shows a node that has valid firmware); and

wherein the first cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the first cell is corrupt (see, for example, paragraph 0025, lines 2-13, which shows that the first node determines that its firmware is outdated) and, upon recognizing that the firmware of the first cell is corrupt, for updating the nonvolatile memory system of the first cell with firmware copied from a cell having valid firmware (see, for example,

paragraph 0027, lines 10-13, which shows that the first node updates its firmware with the valid firmware); and

wherein the second cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the second cell is valid (see, for example, paragraph 0023, lines 7-14, which shows that the second node determines that its firmware is valid); and

wherein the management processor of the second cell has machine readable code to receive an update message via the manageability system interconnect and, in response thereto, to transmit an acknowledgement via the manageability system interconnect (see, for example, paragraph 0023, lines 7-14, which shows that the second cell receives a request for valid firmware and transmits an acknowledgement in response), to enable the high speed interconnect (see, for example, paragraph 0017, lines 14-21, which shows that the high speed interconnect is enabled); and to transmit the firmware in the nonvolatile memory system of the second cell to the first cell via the high speed interconnect (see, for example, paragraph 0027, lines 6-8, which shows that the second node transmits its firmware to the first node).

Goodman in view of Bouchier '343 does not expressly disclose that the firmware is updated because it is corrupt.

However, in an analogous art, Forsman discloses a manageability processor (see, for example, service processor 224 in FIG. 2 and column 3, lines 60-64) that coordinates the operations for updating firmware (see, for example, column 4, lines 2-3). The manageability processor operates even in the event of a system failure (see, for example, column 3, line 64 to column 4, line 1), such as corrupt firmware (see, for example, column 1, lines 24-29). Forsman

discloses recognizing whether the firmware is corrupt (see, for example, column 1, lines 50-55), and recovering the firmware if necessary (see, for example, column 6, lines 16-28).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to update the firmware in Goodman and Bouchier '343 if it is corrupt, such as taught in Forsman, so as to provide for recovery as necessary.

8. Claims 27-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goodman in view of U.S. Patent No. 6,725,317 to Bouchier et al. (now made of record, "Bouchier '317") in view of Forsman.

The Bouchier '317 reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). Again, the examiner anticipates that this rejection will be overcome by a proper showing under 35 U.S.C. 103(c) that the reference is disqualified as prior art in a rejection under 35 U.S.C. 103(a). The Bouchier '317 reference discloses subject matter that is similar to the subject matter disclosed in the Bouchier '343 reference. Accordingly, to expedite prosecution, please refer to the representative claim presented above.

## *Conclusion*

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall whose telephone number is (571) 272-3707. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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